IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences

In re Patent Application of Atty Dkt. 550-299
C# M#

SLOBODNIK et al TC/A.U.: 2138

Serial No. 10/025,816 Examiner: J. Tabone, Jr.

Filed: December 26, 2001 Date: July 31, 2006

Title: METHOD AND APPARATUS FOR MEMORY SELF TESTING

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

☐ **Correspondence Address Indication Form Attached.**

☐ **NOTICE OF APPEAL**
Applicant hereby **appeals** to the Board of Patent Appeals and Interferences from the last decision of the Examiner twice/finally rejecting applicant's claim(s). $500.00 (1401)/$250.00 (2401) $

☐ An appeal **BRIEF** is attached in the pending appeal of the above-identified application $500.00 (1402)/$250.00 (2402) $

☐ Credit for fees paid in prior appeal without decision on merits -$ ( )

☒ A reply brief is attached. **(no fee)**

☐ Petition is hereby made to extend the current due date so as to cover the filing date of this paper and attachment(s)
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Any future submission requiring an extension of time is hereby stated to include a petition for such time extension. The Commissioner is hereby authorized to charge any deficiency, or credit any overpayment, in the fee(s) filed, or asserted to be filed, or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our **Account No. 14-1140.** A duplicate copy of this sheet is attached.

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Serial No. 10/025,816
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For: METHOD AND APPARATUS FOR MEMORY SELF TESTING

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July 31, 2006

Mail Stop Appeal Brief - Patents
Commissioner for Patents
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Alexandria, VA 22313-1450

Sir:

REPLY BRIEF

This Reply Brief is responsive to the Examiner's Answer mailed May 31, 2006.

The Examiner's Answer ignores the teachings of the primary prior art reference (Lo U.S. Patent 5,661,732) and does not respond to the issues raised in Appellants' Appeal Brief. A detailed discussion of each of these new points of argument will follow.

1. Proper construction of Appellants' independent claims 1 and 18

The Examiner's "Response to Argument" on page 11 of the Examiner's Answer recites the definition of "self-test instruction specifying a test methodology" and the Examiner does not appear to take further issue with that definition. Thus, the Examiner appears to acquiesce in Appellants' contention that specifying "a test methodology" requires a sequence of steps and not a single step. Instead of traversing this contention

and/or providing any evidence in support of the Examiner's prior definition of the phrase "test methodology," the Examiner instead on page 12 again attempts to show that the Lo reference teaches such a sequence of steps created by a "single 9-bit word" as alleged by the Examiner.

Thus, as per the Examiner's Answer and in particular the paragraph bridging pages 11 and 12, there is believed an agreement on the Examiner's part that the issue raised in Appellants' Appeal Brief - noting that the Examiner has failed to properly construe the language of Appellants' independent claims - has been mooted and that the Examiner accepts that the language of Appellants' independent claims require a "self-test instruction specifying a test methodology" where the test methodology comprises at least a sequence of steps and not a single step.

2. The Examiner errs again in contending that Lo teaches a single 9-bit word which specifies a "test methodology"

The Examiner liberally quotes from the portion of the Lo patent which defines the 9-bit word from the microcode array 10. As Appellants' noted in the Appeal Brief (last full paragraph on page 11), the Lo reference discloses that each of the 9-bit microcode words includes five different fields, each of which controls a different feature of the processor. The Examiner suggests that each of these features comprises a different step in a series of steps, thereby meeting Appellants' claim definition of "methodology" i.e., a sequence of steps.

The Examiner's conclusion is simply incorrect and this error can be easily shown and understood by reference to Table 8 in column 11 of the Lo reference. A 9-bit word, as the Examiner notes, contains a "Read/Write control field 17" which, as shown in Table 8, can only have a value of zero or one. If the value is zero, it sets the array under test in the Read Mode, and if the value is one, it sets the array under test in the Write Mode. It cannot set the array in test under the Read Mode and then under the Write mode.

As will be clearly understood by those of ordinary skill in the art with respect to self-test systems, Table 8 is a clear admission that each single 9-bit word can only either Read or Write and cannot do both. Thus, in order to initialize or write to the locations in the array under test, it will be necessary for Lo to provide one 9-bit word with read/write control field 17 in the "1" position, i.e., in the "Write" mode to write to all of the elements in the array under test. Subsequently, a second 9-bit word will be needed with read/write control field 17 set to "0", i.e., in the "Read mode" so that the array under test can be read to see whether the information which was previously set in under the "write mode" is correct.

Thus, in the Lo patent, **at least two different** 9-bit words will be needed – one writing to the array under test and the second reading the array under test. Clearly, in accordance with Lo's own teachings, a plurality of words will be needed to define the plurality of steps required for a test methodology. There is no indication in Lo, nor has the Examiner identified any, that will allow a single 9-bit word to specify a sequence of test steps, i.e., a methodology.

The Examiner's misconstruing of the Lo teaching may be appreciated by examining the digits in a 4-digit number, e.g., 1387. While the number 1387 has four places and four different digits, it represents only a single number, 1387. The 1 represents 1000, the 3 represents 3 one hundreds, the 8 represents 8 tens and the 7 represents 7 ones. These four numbers taken together represent the number 1387. There is only a single number specified, even though there are a number of digits.

Similarly, in Lo, there are a number of binary digits in the 9-bit word, but it is still a single word which, at best, contains only a single step. This is why Appellants pointed out previously in the Appeal Brief that Lo has numerous examples of sequences of 9-bit microcode words that are required in order to implement various tests (column 13, lines 7-19, example 4, requires eight 9-bit words to implement "a checkerboard test" and column 15, lines 26-50 specifies two different walking tests, each comprising eight 9-bit microcode words). As disclosed in Lo, all eight of the 9-bit microcode words must be specified in order to implement the "checkerboard test" or either of the two different "walking tests." Thus, Lo fails to teach a single self-test instruction for specifying a test methodology and indeed, in requiring multiple words, teaches away from a single self-test instruction.

3. Appellants appreciate the Examiner's admission that neither Gold nor Correale teach the claim language missing from the Lo reference

On page 16 of the Examiner's Answer, the Examiner impliedly confirms Appellants' contention that the Gold and Correale references do not teach the limitation

of Appellants' independent claims alleged to be missing from the Lo reference. The Examiner relies upon his conclusion that he believes the Lo reference teaches these elements and therefore there is no need for Gold or Correale to contain such a teaching.

Therefore, the strength of the Examiner's argument lies solely on his interpretation of the Lo reference and its purported teaching of a single word which will initiate a test methodology, i.e., a sequence of method steps, which as noted above is simply incorrect.

4. The Examiner alleges that he provides some "reason" or "motivation" for combining the Lo, Gold and/or Correale references

The Examiner's first argument is that "Lo and Gold are analogous arts." The Federal Circuit case of *In re Rouffet* establishes that, even in the case of analogous arts, the burden is on the Examiner to show some reason or motivation for combining the cited prior art references. The Examiner simply may not pick and choose structures or method steps from a plurality of references, even if they are "analogous arts," as this has consistently been held to be prohibited "hindsight." Therefore, the Examiner's argument that Lo and Gold are "analogous arts" does not provide the necessary "reason" or "motivation" for combining references.

Next, the Examiner argues that "combining Lo and Gold clearly solves the problems in [the] claims . . . ." Again, there is no doubt that the combination of the appropriate elements taken from a number of references will solve the problem if combined in the manner of Appellants' claims. However, the test of obviousness is

whether there is some "reason" or "motivation" for picking and choosing those elements and then combining them in the manner of Appellants' claims.

Again, the burden is on the Examiner to show how or why one would have picked various elements from the Lo and Gold or Lo and Correale references. The Examiner has simply failed to provide any reason, other than the fact that, if the elements are combined, they will solve the problem. The Examiner somehow has decided that because the combination of elements will solve the problem, then it must somehow be obvious to pick and choose the elements from these references in order to solve the problem. This circular reasoning by the Examiner has not been supported by any Board or Court of Appeals decision that the undersigned is aware of.

SUMMARY

The Examiner's apparent acquiescence that the claim language requiring that the claimed self-test controller be responsive to a single self-test instruction which specifies a "test methodology" and that test methodology means a plurality of method steps is very much appreciated. The Examiner's contention that the single 9-bit word disclosed in the Lo reference specifies more than a single step in a test methodology is clearly incorrect, as the cited portions of the Lo reference require at least eight separate 9-bit words in order to accomplish any of his listed test methodologies. In fact, no test methodology could be accomplished with the 9-bit words disclosed in Lo because the read/write control field 17 is either in the read mode or the write mode, but cannot be in both at the same time. The Examiner admits that his rejection stands or falls upon the Lo reference teaching a single word specification of a test methodology and provides no legitimate

"reason" or "motivation" for combining the cited prior art references. In effect, the Examiner has acquiesced in two of these four contentions set out in Appellants' Brief and fails to provide support for the two of Appellants' contentions with which he disagrees.

Thus, and in view of the above, the rejection of claims 1-34 under 35 USC §102 or §103 is clearly in error and reversal thereof by this Honorable Board is respectfully requested.

Respectfully submitted,

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